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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/723,655	11/28/2000	Thomas Herman	IR-1986 DIV (2-2500)	6611

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NEW YORK, NY 100368403

EXAMINER

BROCK II, PAUL E

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 07/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/723,655

Applicant(s)

HERMAN, THOMAS

Examiner

Paul E Brock II

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 June 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 9-14, 21 and 22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-14, 21 and 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 9 – 14 and 21 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davies (USPAT 5155052, Davies) in view of Ajit et al. (USPAT 5474946, Ajit).

Davies discloses in figures 1 – 4 the process of manufacturing a MOS gated device.

Davies discloses in figures 1 – 4 forming a gate oxide layer (13) atop a silicon surface (11) of one conductivity type. Davies discloses in figures 1 – 4 forming a layer of polysilicon (14) atop the gate oxide layer. Davies discloses in figures 1 – 4 etching the polysilicon layer and the underlying gate oxide layer into a plurality of spaced stripes (left and right 14 and 13) of oxide and polysilicon overlying the silicon surface. Davies discloses in figures 1 – 4 implanting and diffusing a spaced first base diffusion stripe (12) of the other conductivity type into the silicon surface, using the stripes of oxide and polysilicon as a mask. Davies discloses in figures 1 – 4 implanting and diffusing a source diffusion (15) in to the first base diffusion stripes, using the stripes of oxide and polysilicon as a mask, and leaving invertible channel regions (26) along the outer edges of the first base diffusion stripes. Davies discloses in figures 1 – 4 implanting and diffusing second base diffusion stripes (17) into the silicon surface, using the stripes of oxide

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and polysilicon as a mask, to a depth below that of the source diffusions and extending to the space between the opposite edges of adjacent pairs of the polysilicon stripes. Davies discloses in figures 1 – 4; and column 4, lines 38 – 43 wherein the stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of the first base diffusion stripes, the source diffusions, and the second base diffusions. Davies teaches in figures 1 – 4 and column 3, lines 29 – 30 that the stripes of oxide and polysilicon are spaced 7.5 – 10.5 microns. It is well known in the art to vary dimensions of device features within the same order of magnitude as a matter of design choice, and Ajit teaches in figure 2 and column 29 – 31 stripes which are spaced apart by a gap of about 3 microns. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the spacing of Ajit in the method of Davies in order to use smaller geometries as photolithography techniques improve as stated by Davies in column 3, lines 27 – 33.

With regard to claim 10, Davies teaches in column 3, lines 27 – 30 wherein the polysilicon stripes have a width of 3.1 microns. The combination of Davies (column 3, lines 27 – 33) and Ajit obviously teach wherein the polysilicon stripes have a width of 1.25 microns in order to use smaller geometries as photolithography techniques improve.

With regard to claims 11 and 12, Davies teaches in column 3, lines 47 – 63 wherein the first base diffusions have a depth of 1.25 microns and the source diffusions have a depth of 0.4 microns.

With regard to claim 13, Davies discloses in figures 1 – 4 formation of insulation spacer layers (18) over the top and edges of the polysilicon stripes and the etching of shallow openings through central portions of the source regions and into the first base diffusions and thereafter

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depositing a metal layer (22) over the upper surface of the device to contact the source regions and the first and second base diffusions.

With regard to claim 14, Davies figures 1 – 4 formation of insulation spacer layers (18) over the top and edges of the polysilicon stripes and the etching of shallow openings through central portions of the source regions and into the first base diffusions and thereafter depositing a metal layer (22) over the upper surface of the device to contact the source regions and the first and second base diffusions.

With regard to claim 21, Davies and Ajit further teach that it is obvious wherein the polysilicon stripes are spaced 1.5 microns apart.

With regard to claim 22, Davies and Ajit further teach that it is obvious wherein the polysilicon stripes are spaced 3.2 – 3.4 microns apart.

### ***Response to Arguments***

3. Applicant's arguments filed June 11, 2003 have been fully considered but they are not persuasive.

4. With regard to the applicant's arguments that "Davies teaches forming sidewall spacers 18 before forming low resistivity regions 17," it should be noted that Davies, in column 4, lines 38 – 43, specifically recites the situation where sidewall spacers are not used in implanting the low resistivity regions 17 which correspond to the claimed second base diffusion. Thus Davies teaches in figures 1 – 4; and column 4, lines 38 – 43 the limitation wherein the stripes of oxide

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and polysilicon do not include sidewall spacers during implanting and diffusion of the second base diffusion. Therefore, the arguments are not persuasive, and the rejection is proper.

5. With regard to the applicant's argument that "Davies actually teaches away from using the oxide and polysilicon stripes as a mask in forming the second base regions (low resistivity regions 17)," it should be noted Davies never states that the claimed situation cannot produce a working device. While Davies suggests in column 4, lines 25 – 43 "it has been found that if a thin oxide, analogous to oxide 15 shown in FIG. 1, is used rather than a sidewall spacer 18, insufficient separation between base 12 and low resistivity region 17 is provided, and correspondingly low yields result," it is clear that insufficient separation does not make the device inoperable. Low yields, whether good or bad, do not make Davies teach away from the subject matter. On the contrary, the low yields cited by Davies prove that this method is disclosed and does produce a working device. Therefore, the arguments are not persuasive, and the rejection is proper.

### *Conclusion*

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after

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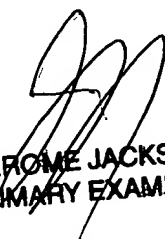
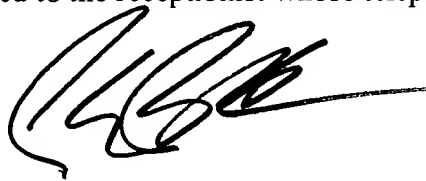
the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II  
July 2, 2003



JEROME JACKSON  
PRIMARY EXAMINER